Features:


Full P1394a Supplement Support includes:
* Arbitrated short reset,
* Multispeed Concatenation,
* Ack Accelerated Arbitration,
* Fly-By Concatenation,
* Programmable Port Disable, Suspend, Resume,
* PHY IDs Do Not Increment Past 63

Provides tree 1394a Fully Compliant Cable Ports at 100/200/400 Megabits per Second (Mb/s)

Single 3.3 V power supply
Logic Performs Bus Initialization and Arbitration Functions
Encode and Decode Functions Included for Data-Strobe Bit-Level Encoding
Incoming Data Resynchronized to Local Clock.
Data Interface to Link-Layer Controller Provided Through 2/4/8 Parallel Lines at 49.152 MHz
24.576 MHZ Crystal Oscillator and PLL Provide TX/RX Data at 100/200/400 Mbps and Link-Layer Controller Clock at 49.152 MHZ.
Cable Power Presence Monitoring.
Programmable Node Power Class Information for System Power Management
Embedded Bus Holder Isolation to Link Layer Controller Interface
Optional On-chip Resistors to Reduce Component Counts for Electrical Isolation to Link Layer Controller Interface
Fully Compliant P1394a 2.0 PHY Map
Separate TPBIAS for Each Port
Fully Interoperable with IEEE Std1394-1995 Devices
Cable Ports Monitor Line Conditions for Active Connection to Remote Node
Self Power Up Reset and Pin less PLL to Reduce Component Counts on System
Supports Windows 98SE/ME/2000 /XP/VISTA