Features:

Compliant with PCI Express Base Specification, Revision 1.1
Integrated 1-Lane PCI Express PHY(2.5Gbps)
Compliant with 1394 Open Host Controller Interface, Specification Revision 1.1

Provides tree 1394a Fully Compliant Cable Ports at 100/200/400 Megabits per Second (Mbit/s)

Logic Performs Bus Initialization and Arbitration Functions
Encode and Decode Functions Included for Data-Strobe Bit-Level Encoding
Incoming Data Resynchronized to Local Clock.
Data Interface to Link-Layer Controller Provided Through 2/4/8 Parallel Lines at 49.152 MHz
24.576 MHZ Crystal Oscillator and PLL Provide TX/RX Data at 100/200/400 Mbps
Cable Power Presence Monitoring.
Programable Node Power Class Information for System Power Management
Embedded Bus Holder Isolation to Link Layer Controller Interface
Optional On-chip Resistors to Reduce Component Counts for Electrical Isolation to Link Layer Controller Interface
Fully Compliant P1394a 2.0 PHY Map
Separate TPBIAS for Each Port
Fully Interoperable with IEEE Std1394-1995 Devices
Cable Ports Monitor Line Conditions for Active Connection to Remote Node
Self Power Up Reset and Pinless PLL to Reduce Component Counts on System
Supports Windows 2000/XP/VISTA